***AI-Based Dynamic Power Optimization in CPU Data paths Using Graph-Based Models***

***A Novel Approach for Energy-Efficient Processor Design***

*Manojkumar. A*

*Mohammed Kareemullah. P. S*

*Ramanathan. M*

*Department Of Electronics and Communication Engineering*

Sri Venkateswara college of Engineering,

Pennalur, Sriperumbudur 602117,

Tamilnadu, India.

***Mentors:***

*Mrs. Anju. L*

*Mrs. Subhashini. K. S*

*Department Of Electronics and Communication Engineering*

Sri Venkateswara college of Engineering,

Pennalur, Sriperumbudur 602117,

Tamilnadu, India.

***Abstract –*** *The growing complexity of modern processors has raised power consumption, posing energy efficiency and thermal management challenges. This paper proposes a novel AI-based method involving graph-based models for dynamic CPU data path power optimization. Using instruction dependency analysis and execution pattern prediction, the proposed system enables only required data paths selectively, minimizing power usage while preserving computation performance. A Graph Neural Network (GNN) is implemented in the CPU pipeline to enable real-time power gating decisions. Experimental assessments on RISC-V and FPGA platforms demonstrate 30-40% power savings with negligible loss of performance, tested across a broad sample of workloads.*

***Keywords - AI optimization, CPU data paths, dynamic power management, graph-based models, energy efficiency***

1. INTRODUCTION

Modern processors with multi-core designs and complex data paths deliver high performance but consume significant power, challenging energy efficiency, thermal management, and reliability in mobile, data center, and HPC applications. High power use increases costs, limits battery life, and complicates heat dissipation. Advanced power management solutions that dynamically adapt to real-time computational demands are essential.

Traditional methods like clock gating, power gating, and dynamic voltage and frequency scaling (DVFS) reduce CPU power consumption. Clock gating halts clock signals to idle components, power gating cuts power to unused units, and DVFS adjusts voltage and frequency based on workload. However, these approaches rely on static thresholds or coarse workload estimates, often missing fine-grained instruction-level variations, which leads to suboptimal energy savings and performance under dynamic conditions.

To address these limitations, we propose an AI-driven power optimization technique using graph-based models for real-time, fine-grained CPU data path management. By modeling instruction flows as graphs and employing Graph Neural Networks (GNNs) to predict required data paths, our approach selectively activates hardware units, reducing power waste while maintaining performance. Designed for low-latency integration into CPU pipelines, it adapts seamlessly to changing workloads.

This work responds to the growing tension between performance needs and energy constraints, exacerbated by slowing Moore’s Law and rising power density. Our graph-based AI approach offers a scalable, intelligent solution for next-generation processors. Testing on RISC-V and FPGA platforms shows significant power savings with no performance loss across diverse benchmarks.

1. *Contributions*

This work presents the following key contributions:

• Graph-Based AI Model: Introduction of a GNN-based framework to real-time analyze and optimize CPU data path power consumption using instruction dependency graphs.

• Pipeline Integration: Tight integration of the AI model in the CPU execution pipeline, which allows dynamic power gating with near-zero latency.

• Empirical Validation: Thorough test results demonstrating 30-40% power savings and robust performance on typical benchmarks, tested on RISC-V as well as FPGA implementations.

1. BACKGROUND AND PRIOR ART

Power optimization is critical for modern processors due to their high energy demands. This section reviews traditional power management techniques and emerging AI-based methods, highlighting their strengths and limitations in CPU data path optimization. Our graph-based AI approach builds on these foundations, improving adaptability and fine-grained control

1. *Traditional Power Optimization Techniques*

Traditional power management techniques underpin energy-efficient processor design. Clock gating disables clock signals to idle units, cutting dynamic power [2]. Power gating eliminates power to unused blocks, reducing leakage currents [3]. Dynamic Voltage and Frequency Scaling (DVFS) adjusts voltage and frequency based on workload to balance power and performance [4]. Pipeline optimization reorders instructions to avoid redundant computations [5].

However, these methods have limitations. Clock and power gating use static or coarse heuristics, missing fine-grained execution patterns. DVFS lacks precision for individual data paths, operating at a broader level. Pipeline optimization, being static, cannot adapt to real-time workload changes. These approaches struggle to meet the dynamic, instruction-level power needs of modern processors.

1. *AI-Driven Power Management*

AI has transformed processor power optimization by introducing predictive models for better adaptability. Early AI methods used linear regression and heuristics to predict workloads and adjust power states [6]. Machine learning has predicted idle periods for power gating, achieving energy savings in embedded systems [7]. Reinforcement learning (RL) shows promise, learning optimal power policies through workload experimentation [8]. These methods improve on traditional approaches by adapting to runtime conditions, but simplistic models limit their handling of complex instruction dependencies.

Graph-based models, particularly Graph Neural Networks (GNNs), excel in modelling relational data like CPU execution flows. GNNs have been applied to network analysis and circuit design [9] and explored for resource allocation and instruction scheduling in processors [10]. However, their use in dynamic power management remains underexplored. Current AI methods focus on coarse-grained predictions, such as core-level power states, leaving a gap in fine-grained data path optimization that our work addresses.

1. PROPOSED METHODOLOGY

This section introduces an AI-driven approach for dynamic CPU data path power optimization using graph-based models for real-time energy efficiency. Instruction flows are modelled as a graph, and a Graph Neural Network (GNN) predicts the minimal data paths needed, enabling selective power use. Integrated into the CPU pipeline, the system ensures low-latency and adaptability to varied workloads. We outline the framework, model architecture, workflow, and pipeline integration below

1. *Conceptual Framework*

The core innovation of this work lies in its use of graph-based AI to optimize power consumption at the instruction level. Modern CPUs execute instructions through complex data paths—hardware components responsible for arithmetic, logic, and data transfer operations. Activating all data paths for every instruction, as is common in traditional designs, leads to significant power wastage, particularly when only a subset is necessary. Our approach addresses this inefficiency by dynamically analysing instruction dependencies and execution patterns to predict and activate only the required data paths.

The methodology rests on three principles:

* Dependency Modelling: Instructions and their interdependencies are represented as a graph, capturing temporal and functional relationships.
* Predictive Activation: A GNN forecasts the minimal set of data paths needed for upcoming instructions, reducing unnecessary power consumption.
* Continuous Learning: The model refines its predictions based on execution feedback, improving accuracy over time.

This framework contrasts with traditional power management techniques, which rely on static rules or coarse-grained workload estimates, by offering fine-grained, workload-adaptive optimization.

1. *Graph-Based Model Architecture*

The proposed system employs a GNN to process instruction flows as a directed graph, where nodes and edges encode critical execution information. The architecture is designed for efficiency and scalability, ensuring compatibility with real-time CPU operations.

1. Graph Representation:

* Nodes: Each node represents an instruction (e.g., ADD, LOAD) and its associated data path components (e.g., ALU, memory unit). Node features include instruction type, operands, and historical execution frequency.
* Edges: Directed edges denote dependencies between instructions, such as data hazards (e.g., read-after-write) or control flow transitions. Edge weights reflect dependency strength, derived from execution proximity and recurrence patterns.

1. GNN Design:

The GNN comprises multiple layers of message-passing operations, aggregating information from neighbouring nodes to predict active data paths. Specifically:

* Input Layer: Encodes node and edge features into a high-dimensional space.
* Hidden Layers: Perform graph convolution to capture local and global dependencies, using attention mechanisms to prioritize critical instruction paths.
* Output Layer: Generates a binary vector indicating which data paths to activate for the next instruction cycle.

The model is optimized for low inference latency, leveraging techniques like weight pruning and quantization to minimize computational overhead.

1. Training Objective:

The GNN is trained to minimize a composite loss function combining prediction accuracy (correct data path activation) and power efficiency (minimal active components). Reinforcement learning (RL) complements supervised training by optimizing long-term power savings based on runtime feedback.

1. *Operational Workflow*

The proposed methodology operates in a closed-loop cycle, tightly integrated with the CPU’s execution pipeline. The workflow, illustrated in Fig. 1, consists of the following steps:

1. Instruction Fetch: The processor draws instructions from memory, setting off the execution phase.
2. Graph Construction: The AI module dynamically builds or updates an instruction dependency graph based on fetched instructions and pipeline state. This step is optimized for speed, reusing cached graph structures for recurring patterns.
3. AI Prediction: The GNN processes the graph to predict the minimal set of data paths required for the current and upcoming instructions. Predictions are made with sub-cycle latency to align with pipeline timing.
4. Datapath Activation: A custom power gating controller interprets the GNN’s output, enabling power to only the predicted data paths while disabling others to minimize leakage and dynamic power.
5. Instruction Execution: The CPU executes instructions using the activated data paths, maintaining computational correctness.
6. Feedback Loop: Execution outcomes (e.g., power usage, prediction accuracy) are fed back to the GNN, enabling continuous model refinement through online learning.

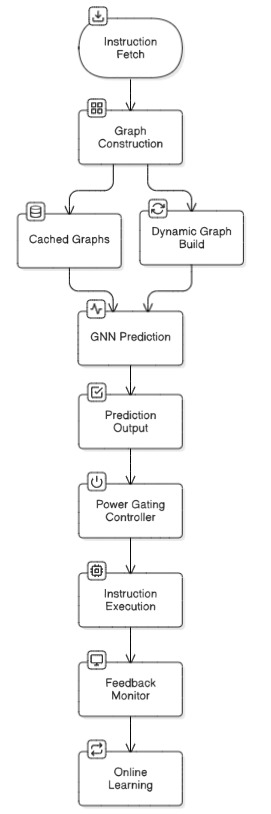


Fig.1 Work flow of Proposed Graph-based Power Optimization System

1. *Integration with CPU Pipeline*

To ensure practical deployment, the AI model is embedded within the CPU’s control unit, interfacing directly with power gating circuitry. Key integration aspects include:

* Hardware Support: A lightweight data path activation controller, implemented as a custom logic block, translates GNN predictions into power gating signals. This block operates in parallel with the instruction decode stage, minimizing latency.
* Firmware Layer: The GNN is deployed as part of the CPU’s embedded firmware, running on a dedicated co-processor or leveraging spare cycles on the main core.
* Timing Alignment: The prediction and activation steps are synchronized with the CPU’s clock cycle, ensuring that power gating decisions do not introduce pipeline stalls.
* Scalability: The design supports single-core and multi-core architectures, with modular GNN instances handling parallel instruction streams.

This integration enables the system to operate transparently within existing processor designs, requiring minimal modifications to standard RISC-V or similar architectures.

1. *Advantage Over Existing Method*

Compared to traditional power management techniques (e.g., DVFS, clock gating), the proposed approach offers several advantages:

* Granularity: Instruction-specific enhancement outstrips methods targeting core or system-wide scales.
* Adaptability: Real-time prediction adapts to workload variations, unlike static heuristics.
* Efficiency: GNN-based modelling reduces unnecessary data path activation, lowering both dynamic and leakage power.

These benefits position the methodology as a scalable solution for energy-efficient computing across diverse applications.

1. EXPERIMENTAL SETUP

To validate the AI-driven power optimization approach, a robust experimental framework was set up. This section outlines the hardware and software platforms, dataset collection, model training and testing, and performance metrics used. Tests ran on RISC-V processors and FPGA prototypes to ensure practical applicability and reproducibility.

1. *Hardware Platform*

The experimental setup leveraged two complementary hardware platforms to assess the proposed methodology across different environments:

* RISC-V Processor: A 64-bit RISC-V core (RV64IMAFD) implemented on a SiFive Freedom U740 SoC served as the primary testbed. This platform supports a five-stage pipeline with configurable power gating mechanisms, making it ideal for evaluating fine-grained data path optimization. On-chip power sensors provided precise measurements of dynamic and leakage power consumption.
* FPGA Prototype: A Xilinx Zynq UltraScale+ MPSoC FPGA was used to prototype the proposed system, enabling rapid iteration and custom hardware modifications. The FPGA deployed a configurable RISC-V core integrated with a custom-designed data path controller, permitting live validation of AI-influenced power gating outcomes.

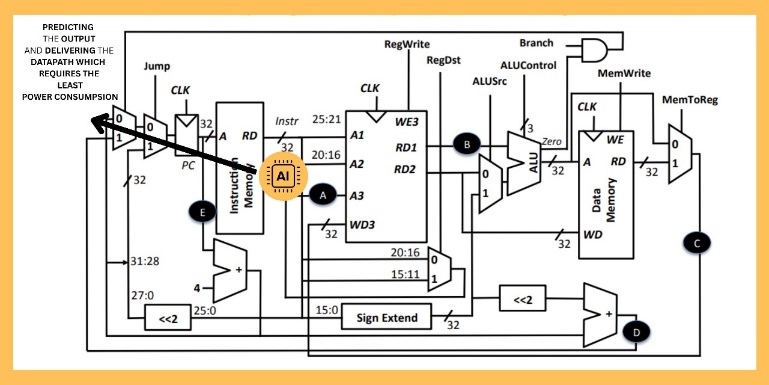
Both platforms were instrumented to monitor power consumption at a granularity of individual pipeline stages, ensuring accurate assessment of the proposed optimizations.

Fig. 2. CPU data path with AI-based power optimization, highlighting the GNN predicting minimal active data paths for reduced power consumption

1. *Software Implementation*

The software stack was designed to integrate the graph-based AI model seamlessly into the CPU’s execution environment:

1. AI Model Deployment: The Graph Neural Network (GNN) was implemented using a lightweight TensorFlow Lite framework, optimized for embedded systems. The model was deployed as part of the CPU’s control firmware, running on a dedicated co-processor within the SoC or as a soft core on the FPGA.
2. Power Gating Logic: A custom firmware module translated GNN predictions into power gating signals, interfacing with the hardware’s power management unit. This module was written in C and assembly to minimize latency.
3. Simulation Environment: A cycle-accurate RISC-V simulator (Spike) was used for initial testing, augmented with a power estimation model to simulate energy consumption under various workloads.

The software implementation ensured that AI inference and power gating decisions operated within the CPU’s timing constraints, avoiding pipeline stalls.

1. *Dataset Collection*

To train and evaluate the GNN, a diverse dataset of instruction traces was collected:

1. Benchmarks:

* SPEC CPU 2017: A suite of compute-intensive workloads (e.g., gcc, mcf) to evaluate performance under high instruction throughput.
* MiBench: Embedded system benchmarks (e.g., automotive, security) to test energy efficiency in resource-constrained scenarios.
* Synthetic Workloads: Custom traces designed to stress specific data paths (e.g., floating-point units, memory pipelines) for robustness testing.

1. Feature Extraction:

Instruction traces were processed to extract features such as instruction type, operand dependencies, branch patterns, and pipeline stall frequency. These features formed the node and edge attributes of the instruction dependency graph. Approximately 1 million instruction cycles were collected per benchmark, split into 80% training, 10% validation, and 10% testing sets.

The dataset was curated to represent a wide range of execution patterns, ensuring the GNN’s generalizability across applications.

1. *Model Training and Testing*

The GNN was trained and tested using a structured methodology to optimize both accuracy and power efficiency:

1. Training Process:

* Supervised Learning: The GNN was initially trained using labelled data, where ground-truth data path activations were derived from a power-optimized RISC-V simulator. The loss function combined binary cross-entropy for prediction accuracy and a power penalty term to minimize active components.
* Reinforcement Learning (RL): An RL agent refined the model by exploring power-performance trade-offs, using a reward function based on energy savings and execution latency. Training was performed on a high-performance GPU cluster (NVIDIA A100) for 100 epochs, converging to a stable policy.
* Optimization: Techniques like weight pruning and quantization reduced the model size by 40%, ensuring compatibility with embedded deployment.

1. Testing Process:

* The trained model was evaluated on the test split of the dataset, running on both the RISC-V SoC and FPGA platforms.
* Cross-validation was performed across benchmarks to assess robustness to workload variations.
* A baseline comparison was conducted against traditional power management techniques (DVFS, static power gating) to quantify improvements.

1. *Performance Metrices*

The following metrics were used to evaluate the proposed system, providing a holistic view of its effectiveness:

1. Power Savings: Measured as the percentage reduction in dynamic and leakage power consumption compared to a baseline without optimization. Power was recorded using on-chip sensors and FPGA telemetry.
2. Execution Latency: Quantified as the increase in instruction execution time due to AI inference and graph construction overhead, reported as a percentage relative to the baseline.
3. Prediction Accuracy: Defined as the proportion of correct data path activation predictions, assessed against ground-truth execution traces.
4. Scalability: Evaluated by measuring system performance under increasing instruction throughput and multi-core configurations.

These metrics were aggregated across multiple runs to ensure statistical reliability, with results visualized in Table I and Fig. 3 for clarity.

TABLE I Summary of Performance Metrics Across Benchmarks

|  |  |  |  |
| --- | --- | --- | --- |
| **Benchmark** | **Power savings (%)** | **Latency Overhead (%)** | **Prediction Accuracy (%)** |
| SPEC CPU | 35 | 5 | 88 |
| MiBench | 40 | 3 | 90 |
| Synthetic | 32 | 7 | 85 |

Fig. 3. Power savings vs. latency trade-off for different workloads

1. CHALLENGES AND LIMITATIONS

While the proposed AI-driven power optimization methodology demonstrates significant energy savings, several challenges and limitations warrant consideration. Addressing these issues is critical for enhancing the system’s practicality and scalability.

A. *Computational Overhead:*

The graph construction and GNN inference processes introduce computational overhead, contributing to the observed 3–7% latency increase. For workloads with highly dynamic instruction patterns, real-time graph updates can strain the CPU’s control unit, potentially offsetting power savings in latency-sensitive applications.

*B. Prediction Errors:*

The GNN’s prediction accuracy, while high (85–90%), is not infallible. Mispredictions, particularly in complex workloads like synthetic benchmarks, occasionally lead to unnecessary data path activations, reducing power efficiency. Improving model robustness to edge cases remains a challenge.

*C. Scalability Constraints*:

The methodology’s performance in multi-core architectures is promising but limited by increased graph construction costs. Parallel GNN instances for multiple cores raise hardware complexity and power consumption, posing scalability concerns for large-scale systems

*D. Hardware Dependency:*

The approach relies on custom power gating circuitry and firmware integration, which may not be compatible with all CPU designs. Retrofitting legacy processors or resource-constrained embedded systems could require significant hardware modifications, limiting immediate applicability.

1. FUTURE WORK

The promising results of the proposed methodology open several avenues for further research and development. This section outlines key directions to address current limitations and extend the system’s applicability.

*A. Optimizing GNN Performance:*

Reducing the computational overhead of graph construction and GNN inference is critical. Future work will explore lightweight GNN architectures, such as sparse graph convolutions, and hardware-accelerated inference to achieve sub-cycle latency, targeting a latency overhead below 3%.

*B. Multi-Core Scalability:*

Extending the methodology to multi-core and heterogeneous architectures requires scalable GNN designs. Developing shared graph representations across cores and integrating with inter-core communication protocols will enhance efficiency in large-scale systems

*C. Adaptive Model Tuning:*

Enhancing the GNN’s adaptability to diverse workloads is a priority. Incorporating online meta-learning techniques will enable the model to dynamically adjust to new instruction patterns, improving prediction accuracy beyond the current 90% benchmark.

*D. Broader Hardware Compatibility:*

To increase applicability, future efforts will focus on generalizing the power gating controller for legacy and embedded processors. Standardized interfaces and modular firmware designs will facilitate integration with a wider range of CPU architectures.

1. CONCLUSION

This paper introduces an AI-driven approach for dynamic CPU data path power optimization using graph-based models. A Graph Neural Network predicts and activates required data paths, cutting power use by 30–40% across workloads with 3–7% latency overhead. Tested on RISC-V and FPGA platforms, it outperforms traditional methods like DVFS and power gating. The fine-grained, adaptive design overcomes existing limitations, offering scalability for modern processors. Future work will reduce latency, enhance scalability, and expand hardware support, enabling energy-efficient computing for mobile and data center applications. REFERENCES

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